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STANDARD OMNIPOINT INTERFACE

Preliminary System Documentation

July 7, 1975.

STANDARD OMNIPORT INTERFACE

Purpose:

The omniport interface is the basic building block for all omniport peripheral interface boards. It decodes omniport signals and makes them available to the device interface and encodes signals for the omniport generated by the device interface.

Signal Description:

To Device Interface:

RESET
SEL
SCOS
SGSI
SDOS
SGDI
D0-7

CLK

SYNC2
+5V
-12V

From Device Interface:

DATA0-7
STATUS0-7
CSENB
START

RESET:

True during system reset time. This signal should be used to do any initialization appropriate for the device. This signal is also true during power-up.

SEL:

True when the interface has been addressed. This signal is reset when another interface is addressed.

SCOS:

Device command strobe ($SEL \wedge COS$). The command is present on data lines D0-7.

SGSI:

Device status strobe ($SEL \wedge GSI$). The status should be present on data lines STATUS 0-7.

SDOS:

Data output strobe ($SEL \wedge DOS$). The data to be output to the device is present on data lines D0-7.

SGDI:

Data input Strobe ($SEL \wedge GDI$). The data from the device should be present on data lines DATA0-7.

Operation:

When the system is started, or the interface is powered on, a RESET is generated and the interface is deselected.

In order to activate the interface, it must be addressed by presenting the Device Address on the omniport data lines concurrent with an Address Out Strobe. This must be followed by a Gate Status In, which returns the Answer-Back code for the device. At termination of the first Gate Status In after the interface has been addressed, SEL comes true, and the interface is then active.

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Any subsequent RESET or Address Out Strobe deselects the interface. If the interface is re-addressed, it will become reselected after the next Gate Status In.

Device Address:

The device address is set by two jumper plugs in the interface. It can be wired in directly or directed to an external device such as a thumbwheel switch.

Device Answer-Back Code:

This code is wired into the interface (refer to the schematic for the standard omniport interface). Its purpose is to inform the system as to the nature of the device being addressed.

Clock Signals:

Two clock signals are available from the system: a $1.25\ \mu\text{s}$ clock called SYNC 2, and a $5\ \mu\text{s}$ clock called CLK. These signals are enabled by grounding CSENB. CSENB is normally high, so that the clock signals do not cause the interface to draw any power.

Start Signal:

This is a 12V CMOS level which, when grounded, starts the main system.

Power:

Two voltages are available from the interface for use by other equipment on the board: +5V and -12V. Both are fused at 250 ma and Zener protected.

Interface:

All interface lines are 5-volt CMOS levels. These are TTL compatible. All output lines will drive one standard TTL load. Timings are given on the accompanying diagram.

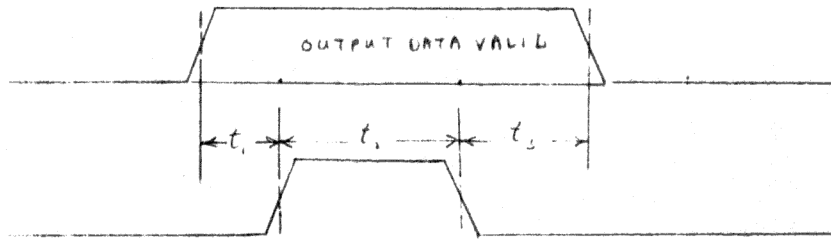
Protection:

All lines between the interface and the Omniport connector are protected against over voltage, so that a fault on the interface board will not propagate destructively either to the main system or to other interfaces on the Omniport.

OMNIPORT TIMINGS

DO-7

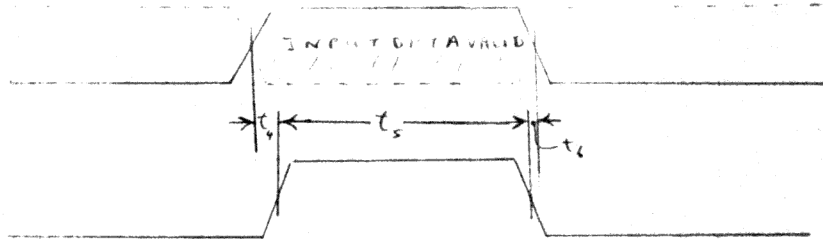
SCOS, SDOs



	min	nom	max
t ₁		0.8 μ s	
t ₂		1.8 μ s	
t ₃		1.3 μ s	

DATA 0-7
STATIS 0-7

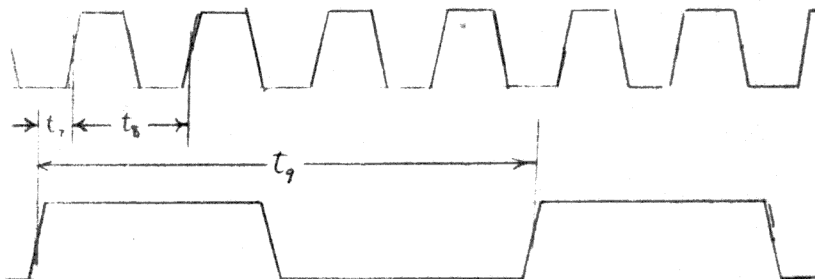
SGSI, SGDI



	min	nom	max
t ₄			
t ₅		2.6 μ s	
t ₆	0	-	-

SYNC 2

CLK



	min	nom	max
t ₇		0.3 μ s	
t ₈		1.25 μ s	
t ₉		5 μ s	